TOSHIBA

Embedded RISC microcontroller for high end automotive applications

TX19A50 Family

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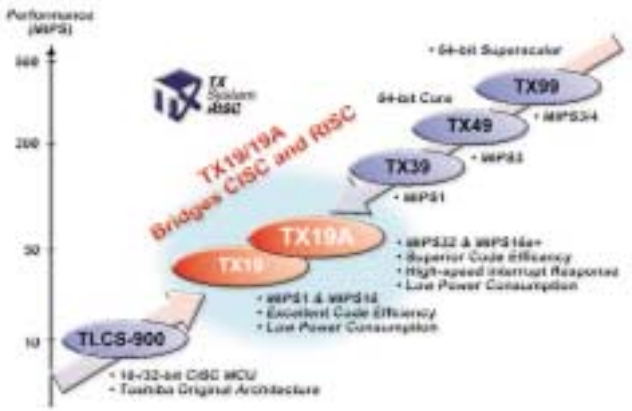
The TX19A Core

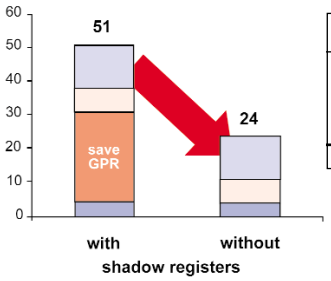
Toshiba offers a huge line-up of processor cores, ranging from low-cost CISC microcontrollers to powerful 64-bit superscalar RISC processors. TX19A is our latest state-of-the-art core that bridges these two worlds. On one hand it provides the calculation power of a 32-bit RISC core with a single cycle MAC unit, while simultaneously being a very compact and cost effective core. Its best in class code efficiency, very fast interrupt response and context switching, as well as high integration of peripherals and memory, makes it ideal for high-end embedded automotive systems.



Key Features of TX19A

- Up to 64 MHz operation speed
- Single-cycle MAC for fast calculation (32b x 32b + 64b)
- 8 built-in register-banks for high speed interrupt handling
- Based on the MIPS™ standard architecture
- Additional 16-bit instruction set for minimum code size
- Embedded Mask & Flash technology
- ROM correction function for mask derivatives
- Two fast A/D converters with 8 channel each: 3μs converter sampling rate + safety supervision function
- Window watchdog for internal supervision
- High performance communication units (SPI) with FIFO
- Special Boot ROM mode for secure in-field re-programming via CAN

Fast Interrupt Response by Shadow Registers



Interrupt Response Time (clock cycles)	shadow registers without	with
Jump to exception handler	4	4
Save GPR	27	-
Save HI/LO, EPC	7	7
Save Stat. Reg., Read End Adr., Jump to End Adr., Enable Interrupt	13	13
TOTAL	51	24

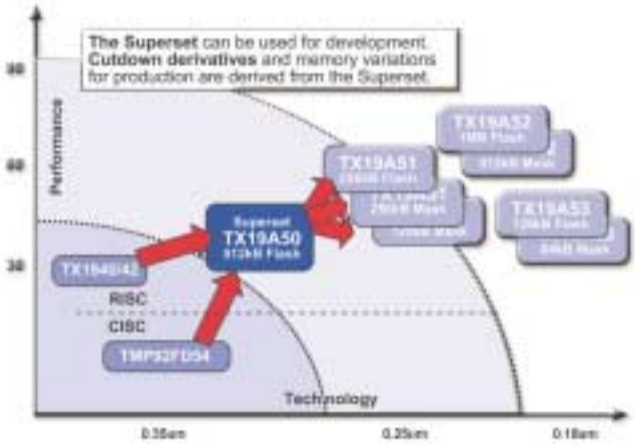
8 built-in register banks removes the necessity to save the GPR by software. This halves the interrupt response time.

The Superset Concept

Using the TX19A core Toshiba developed a superset MCU called TX19A50, which is dedicated to automotive applications with hard real-time and strict fail-safe requirements such as airbag, car radio and instrument clusters. The superset MCU embeds a large number of peripherals to cover almost every possible application in those areas. It is therefore ideal for evaluation & development purposes. Not only that, it is possible to derive a series of cut-down derivatives from the superset MCU allowing use in a host of mass production applications. This approach allows an immediate start to development with maximum flexibility while always providing a cost-optimised solution.

The TX19A50 Superset MCU was developed by Toshiba's European Automotive Design centre in Düsseldorf, Germany and is available today.

TX19A Product Roadmap



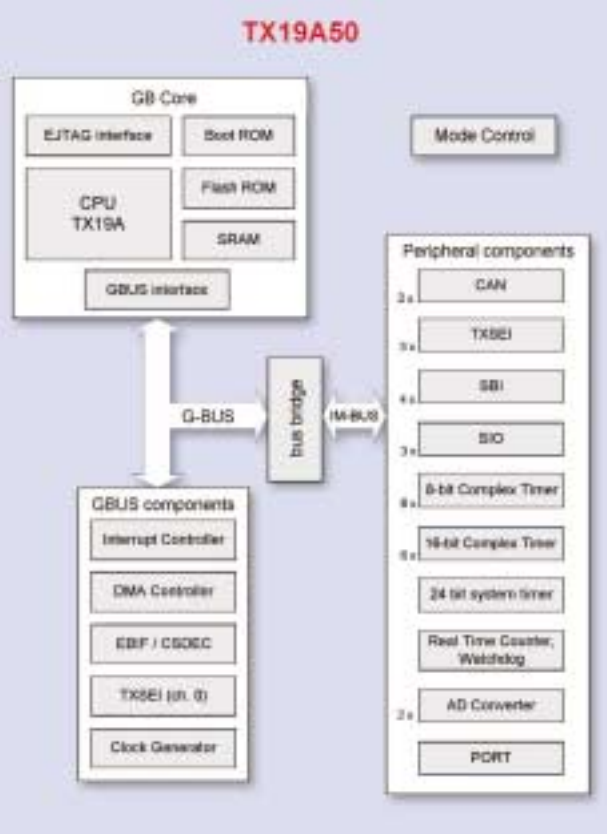
TX19A50 Superset Features

Built-in TX19A Core:
- Toshiba-developed TX19A core based on MIPS R3000A architecture
- Extended MIPS32, MIPS16e and MIPS16e+ instruction set
- MAC function: 1clock (32b x 32b +64b)
- Register window function to switch between different general-purpose-register banks for fast interrupt service
- EJTAG interface including PC tracing and data tracing
- Non maskable interrupt (NMI)
- Little-endian coding

Memory:
- 512 kbyte internal Flash-ROM including interleave mode (0 wait cycles), slow-mode capability to work at 32 kHz
- 32 kbyte internal SRAM (0 wait cycles)
- 8 kbyte internal Boot-ROM
- External Bus Interface (EBIF) for connecting asynchronous RAM/ROM or external ASICs (8 or 16 bit data bus, multiplexed data/address lines)

Peripheral Controllers:
- Two A/D converter with 10-bit resolution, a sample time of 3μs, an 8-to-1 input multiplexer and automatic full-scan capability
- DMA controller (DMAC), 8 channels
- Interrupt Controller (IRC), handling of up to 95 interrupt sources, 7 priority level settable for each interrupt source, 11 external interrupt lines
- 8-bit complex timer – 8 channels, PWM / PPG mode, output frequency generation (max. 8 MHz)
- 16-bit complex timer – 6 channels, PWM / PPG mode, frequency/time measurement mode
- 24 bit System Timer, read-on-the-fly capability
- Watchdog Timer with time-out and time-window function
- Real Time Clock, including a LED-blinking timer with brightness control
- Serial interface (SIO) –3 channels, UART mode, synchronous mode
- Synchronous serial interface (TXSEI) - 4 channels, SPI compatible, up to 8Mbit/s transfer rate
- CAN-bus controller (TXCAN), 2 channels, 16 mailboxes each
- Serial Bus Interface (SBI) – 4 channels, I²C mode (400 kbit/s), SIO mode
- General Purpose I/O´s (PORT)

Miscellaneous:
- 40 MHz maximum operating frequency
- -40°C to 85°C operating ambient temperature
- 100 pin QFP package (144 pin bonding option for superset device)
- 3.3 V power supply voltage
- Integrated voltage regulator for 2.5 V core voltage supply
- 5V tolerant I/Os on dedicated signals
- Built-in clock generator with PLL x 4
- Built-in 32 kHz-low-speed clock generator for real time clock and supervision-circuit
- On/off key wake-up logic
- Cold/warm start recognition to distinguish power-on-reset and reset during normal operation



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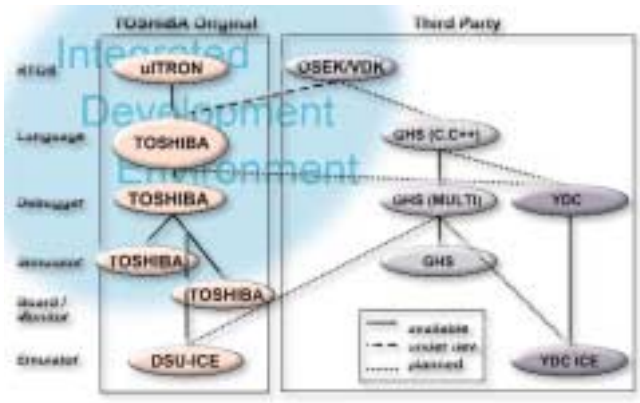
Development Tools

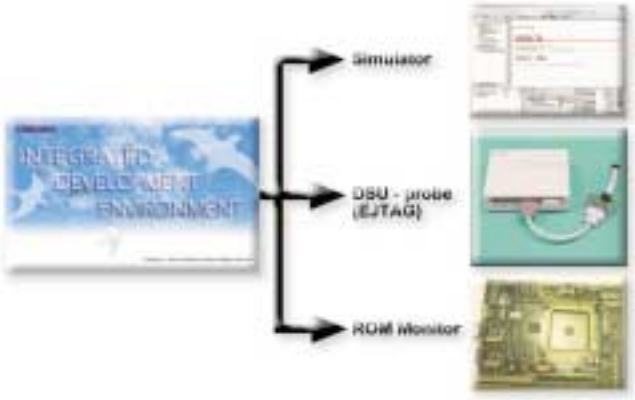
A state-of-the-art development tool set for TX19A is available from Toshiba and third party companies. The new TX19A core and compiler was developed with special attention to code density and it achieves best-in-class code size results.
Development, debugging and flash programming is possible via the low-cost EJTAG DSU-probe. With the simulator software development can start even before your target hardware is available and by using the ROM monitor, debugging is possible even without an in-circuit emulator.

The standard automotive RTOS OSEK is available from third party vendors. For the TX19A50 an evaluation board is available to evaluate the performance even before your target system is available.

Tools Chain Plan for the TX19A



TX19A Development Tools



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